

CMOS Dual 64-Stage Static Shift Register

CD4517B Types

High-Voltage Types (20-Volt Rating)

■ CD4517B dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the CD4517B. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

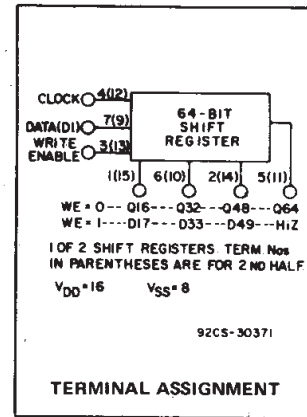
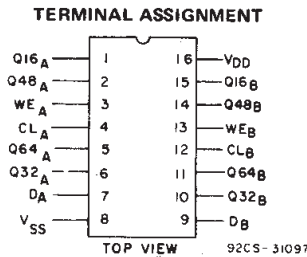
The CD4517B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Low quiescent current – 10 nA/pkg (typ.) at $V_{DD} = 5\text{ V}$
- Clock frequency 12 MHz (typ.) at $V_{DD} = 10\text{ V}$
- Schmitt trigger clock inputs allow operation with very slow clock rise and fall times
- Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads
- Three-state outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Time-delay circuits
- Scratch-pad memories
- General-purpose serial shift-register applications



MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|--|--|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | -0.5V to +20V |
| Voltages referenced to V_{SS} Terminal) | |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to $V_{DD} + 0.5\text{ V}$ |
| DC INPUT CURRENT, ANY ONE INPUT | $\pm 10\text{ mA}$ |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ | 500mW |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ | 100mW |
| OPERATING-TEMPERATURE RANGE (T_A) | -55°C to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | -65°C to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max | $+265^\circ\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|------|-------|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$) | 3 | 18 | V |

TRUTH TABLE

| Clock | Write Enable | Data | Stage 16 Tap | Stage 32 Tap | Stage 48 Tap | Stage 64 Tap |
|-------|--------------|-------|--------------|--------------|--------------|--------------|
| 0 | 0 | X | Q16 | Q32 | Q48 | Q64 |
| 0 | 1 | X | Z | Z | Z | Z |
| 1 | 0 | X | Q16 | Q32 | Q48 | Q64 |
| 1 | 1 | X | Z | Z | Z | Z |
| ~ | 0 | DI In | Q16 | Q32 | Q48 | Q64 |
| ~ | 1 | DI In | D17 In | D33 In | D49 In | Z |
| ~ | 0 | X | Q16 | Q32 | Q48 | Q64 |
| ~ | 1 | X | Z | Z | Z | Z |

X = Don't Care

Z = High Impedance

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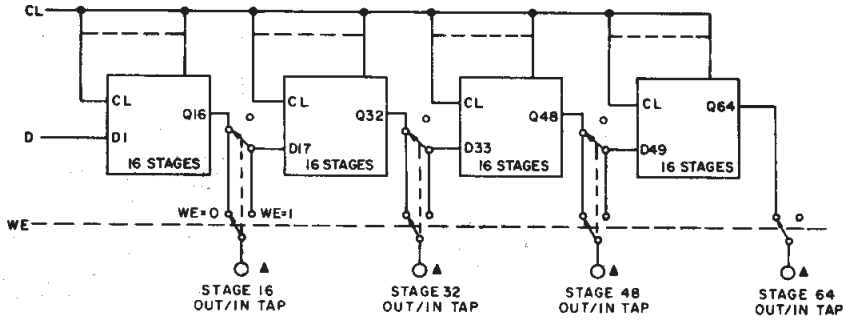


Fig. 1—CD4517B functional block diagram (one half).

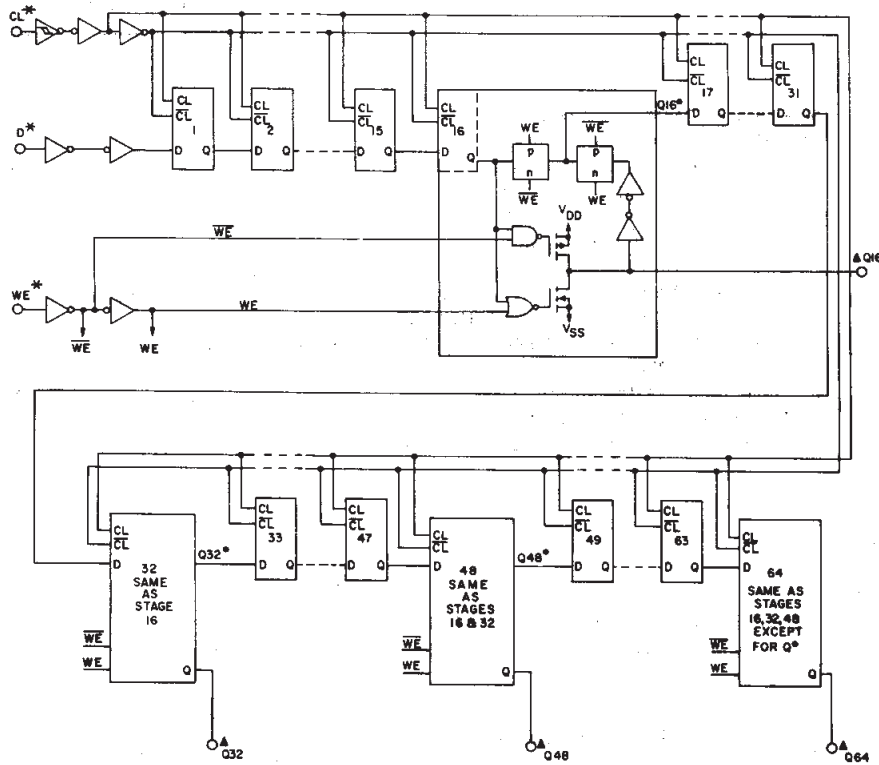


Fig. 2—CD4517B logic block diagram (one half).

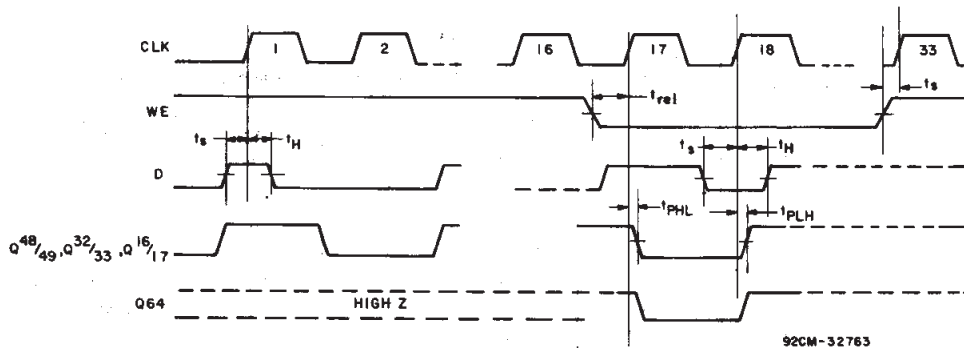


Fig. 3—Dynamic test waveforms.

CD4517B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0,5 | 5 | 5 | 5 | 150 | 150 | - | 0,04 | 5 | μA |
| | - | 0,10 | 10 | 10 | 10 | 300 | 300 | - | 0,04 | 10 | |
| | - | 0,15 | 15 | 20 | 20 | 600 | 600 | - | 0,04 | 20 | |
| | - | 0,20 | 20 | 100 | 100 | 3000 | 3000 | - | 0,08 | 100 | |
| Output Low (Sink) Current I _{OL} Min. | 0,4 | 0,5 | 5 | 0,64 | 0,61 | 0,42 | 0,36 | 0,51 | 1 | - | mA |
| | 0,5 | 0,10 | 10 | 1,6 | 1,5 | 1,1 | 0,9 | 1,3 | 2,6 | - | |
| | 1,5 | 0,15 | 15 | 4,2 | 4 | 2,8 | 2,4 | 3,4 | 6,8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4,6 | 0,5 | 5 | -0,64 | -0,61 | -0,42 | -0,36 | -0,51 | -1 | - | mA |
| | 2,5 | 0,5 | 5 | -2 | -1,8 | -1,3 | -1,15 | -1,6 | -3,2 | - | |
| | 9,5 | 0,10 | 10 | -1,6 | -1,5 | -1,1 | -0,9 | -1,3 | -2,6 | - | |
| | 13,5 | 0,15 | 15 | -4,2 | -4 | -2,8 | -2,4 | -3,4 | -6,8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0,5 | 5 | 0,05 | | | - | 0 | 0,05 | - | V |
| | - | 0,10 | 10 | 0,05 | | | - | 0 | 0,05 | - | |
| | - | 0,15 | 15 | 0,05 | | | - | 0 | 0,05 | - | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0,5 | 5 | 4,95 | | | 4,95 | 5 | - | - | V |
| | - | 0,10 | 10 | 9,95 | | | 9,95 | 10 | - | - | |
| | - | 0,15 | 15 | 14,95 | | | 14,95 | 15 | - | - | |
| Input Low Voltage V _{IL} Max. | 0,5, 4,5 | - | 5 | 1,5 | | | - | - | 1,5 | - | V |
| | 1,9 | - | 10 | 3 | | | - | - | 3 | - | |
| | 1,5, 13,5 | - | 15 | 4 | | | - | - | 4 | - | |
| Input High Voltage V _{IH} Min. | 0,5, 4,5 | - | 5 | 3,5 | | | 3,5 | - | - | - | V |
| | 1,9 | - | 10 | 7 | | | 7 | - | - | - | |
| | 1,5, 13,5 | - | 15 | 11 | | | 11 | - | - | - | |
| Input Current I _{IN} Max. | - | 0,18 | 18 | ±0,1 | ±0,1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0,1 | μA |
| 3-State Output Leakage Current I _{OUT} Max. | 0,18 | 0,18 | 18 | ±0,4 | ±0,4 | ±12 | ±12 | - | ±10 ⁻⁴ | ±0,4 | μA |

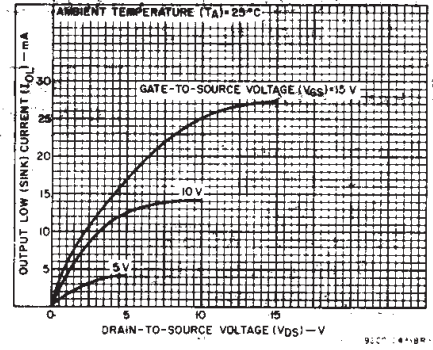


Fig. 4—Typical n-channel output low (sink) current characteristics.

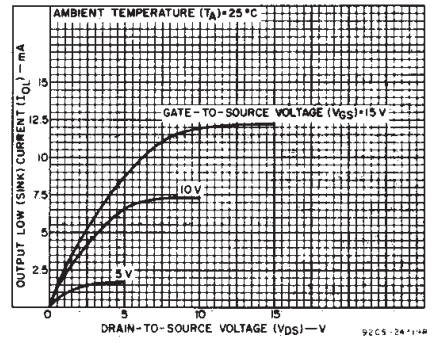


Fig. 5—Minimum n-channel output low (sink) current characteristics.

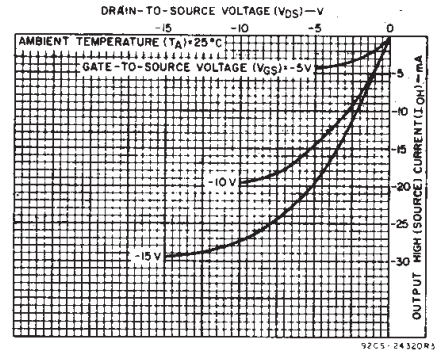


Fig. 6—Typical p-channel output high (source) current characteristics.

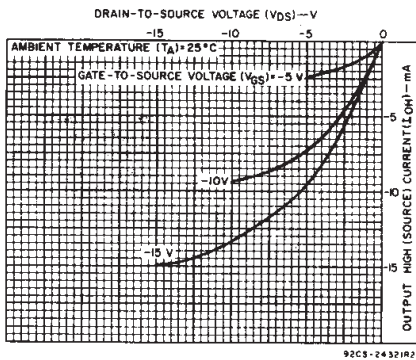


Fig. 7—Minimum p-channel output high (source) current characteristics.

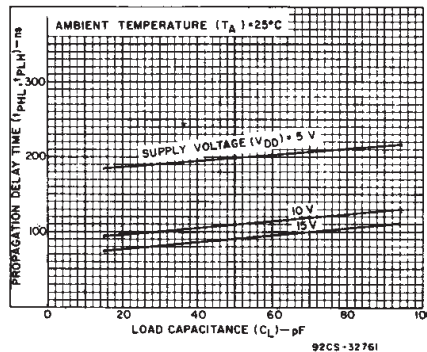


Fig. 8—Typical propagation delay time as a function of load capacitance.

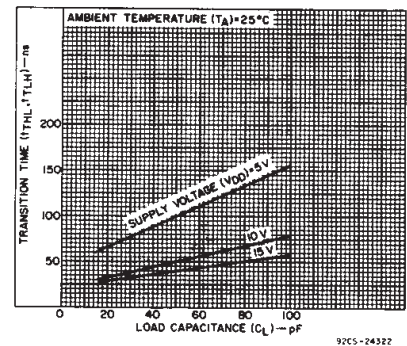


Fig. 9—Typical transition time as a function of load capacitance.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | V _{DD} (V) | LIMITS | | | UNITS |
|---|-----------------|---------------------|-----------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| Propagation Delay Time: CL to Bit 16 Tap t _{PHL} , t _{PLH} | | 5 | — | 200 | 400 | ns |
| | | 10 | — | 110 | 220 | |
| | | 15 | — | 90 | 180 | |
| 3-State Output, WE to Bit 16 Tap t _{PZH} , t _{PLZ} ; t _{PZH} , t _{PZL} (See Note) | | 5 | — | 75 | 150 | ns |
| | | 10 | — | 40 | 80 | |
| | | 15 | — | 30 | 60 | |
| Output Transition Time t _{THL} , t _{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Write Enable-to-Clock Setup Time | | 5 | 0 | -50 | — | ns |
| | | 10 | 0 | -25 | — | |
| | | 15 | 0 | -15 | — | |
| Data-to-Clock Setup Time, t _s | | 5 | 20 | 0 | — | ns |
| | | 10 | 10 | 0 | — | |
| | | 15 | 10 | 0 | — | |
| Minimum Write Enable-to-Clock Release Time | | 5 | — | 50 | 100 | ns |
| | | 10 | — | 25 | 50 | |
| | | 15 | — | 20 | 40 | |
| Minimum Data-to-Clock Hold Time, t _H | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 25 | 50 | |
| Minimum Clock Pulse Width, t _W | | 5 | — | 90 | 180 | ns |
| | | 10 | — | 40 | 80 | |
| | | 15 | — | 25 | 50 | |
| Maximum Clock Input Frequency, f _{CL} | | 5 | 3 | 6 | — | MHz |
| | | 10 | 6 | 12 | — | |
| | | 15 | 8 | 15 | — | |
| Maximum Clock Input Rise or Fall Time, t _{rCL} , t _{fCL} | | 5 | UNLIMITED | | | μs |
| | | 10 | | | | |
| | | 15 | | | | |
| Input Capacitance C _{IN} | Any Input | | — | 5 | 7.5 | pF |

NOTE: Measured at the point of 10% change in output with an output load of 50 pF, R_L = 1 kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L = 1 kΩ to V_{SS} for t_{PZH}, t_{PHZ}.

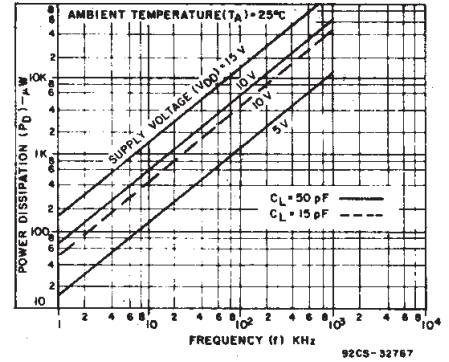


Fig. 10—Typical power dissipation as a function of frequency.

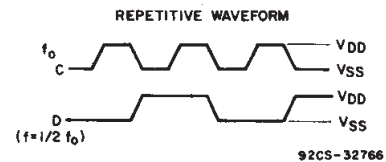
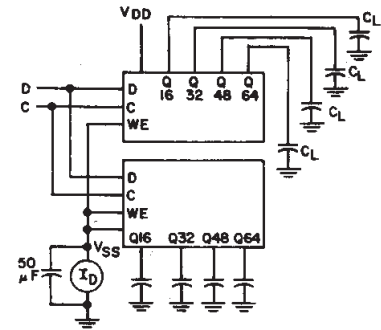


Fig. 11—Dynamic power dissipation test circuit and waveforms.

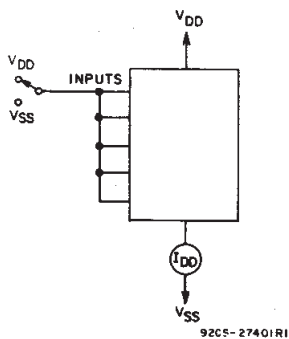


Fig. 12—Quiescent device current test circuit.

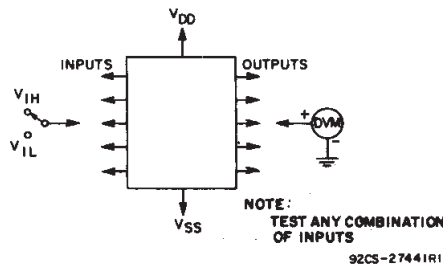


Fig. 13—Input voltage test circuit.

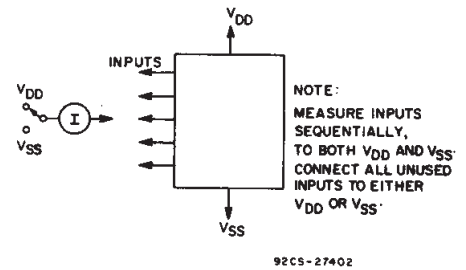
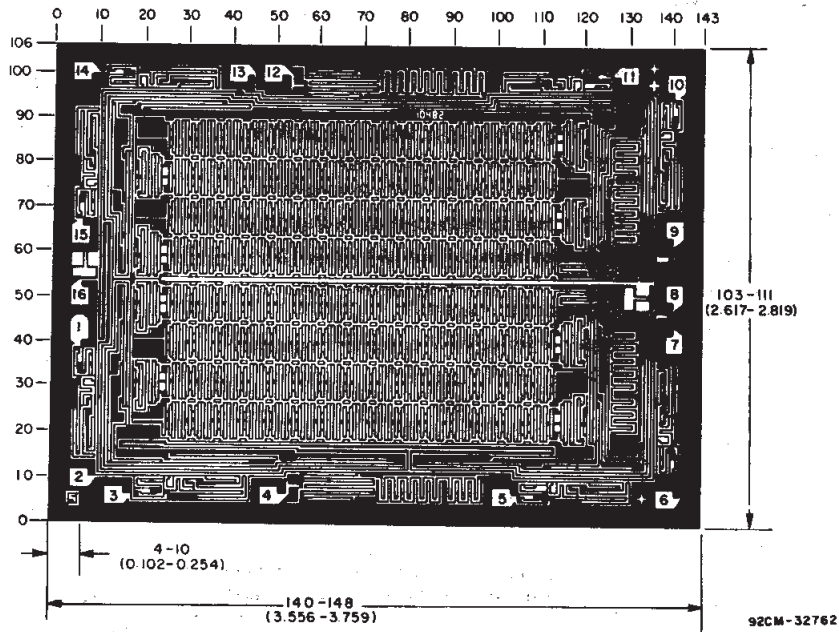


Fig. 14—Input current test circuit.

CD4517B Types



Dimensions and pad layout for CD4517B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4517BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4517BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4517BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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